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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/484,311	01/18/2000	James John Casto	1001-0087	9539

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EXAMINER
LEE, EUGENE

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/484,311	Applicant(s) CASTO ET AL.	
	Examiner Eugene Lee	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-12,15-25 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-12,15-25 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

The finality of the Office Action mailed 7/3/02 is withdrawn in view of the response filed 10/3/02.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 2 thru 5, 10, 11, 17, 18, 22 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by MacPherson et al. '437 B1. MacPherson discloses (see, for example, Figure 1) fuses formed for an integrated circuit die in a semiconductor package. Fuse (programmable element) 1 is coupled to a signal line (power supply voltage node). A second fuse (second programmable element) 3 is coupled to a different signal line (second power supply voltage node). A middle fuse has two nodes (internal package

node) that couple a second end of fuse 1 to a second end of fuse 3. A photoresist layer 21 covers the fuse.

3. Claims 2, 7 thru 9, 11, 12, 15 thru 18, 20 thru 23 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Crafts et al. '968. Crafts discloses (see, for example, FIG. 3) a fuse array comprising fuse structures 10 wherein a first and second end is coupled to V_{DD}, external I/O terminals or resistors 40. Memory devices (such as PROMs) are conventionally placed in dies in semiconductor packages such as those found on a computer motherboard, etc. In FIG. 3, there are two fuses 10 that lie on a fourth row of the PROM fuse array. Each fuse is coupled to a different V_{DD} power supply. A second end of one of the fuses 10 is coupled to a second end of the other fuse 10 by way of a node (black dot, internal package node).

4. Claims 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamdy et al. '829. Hamdy discloses (see, for example, FIGURE 5a) anti-fuses formed for a integrated circuit die in a semiconductor package. Anti-fuse (programmable element) 168d is coupled to a bit line (power supply voltage) 00. Anti-fuse (another programmable element) 168h is coupled between a second end of anti-fuse 168d and output (external package connection) 178.

5. Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Best '031. Best discloses (see, for example, FIG. 2) a circuit comprising a fuse (one-time programmable element) 255, V_{SS} (power supply voltage node), fuse (another one-time programmable element) 245, and external pad (external package connection) 260. A node (internal package node) lies adjacent to pad 265 in between pads 245, 255.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacPherson et al. '437 B1. MacPherson discloses the claimed invention except for the programmable element being not covered by a protective layer. It would have been obvious to one of ordinary skill in the art at the time of invention was made to exclude the protective layer, since it has been held that omission of an element and its function in a combination where the remaining elements perform the same function as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

8. Claims 19 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacPherson et al. '437 B1 as applied to claims 2 thru 5, 10 and 11, 17, 18, 22 and 23 above, and further in view of Hall '632 B1. MacPherson does not disclose the integrated circuit die including a processor wherein the processor is programmed (to perform various functions) by programmable elements. However, Hall discloses (see, for example, FIG. 3) a fuse array 202, 204, 206, a processor and clock source. Hall discloses that the fuse array specifies the operating characteristics of the processor (i.e. clock frequency). Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the fuses of Macpherson in order to specify the operating characteristics of a processor.

9. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacPherson et al. '437 B1 as applied to claims 2 thru 5, 10 and 11, 17, 18, 22 and 23 above, and further in view of Barth, Jr. et al. '616. MacPherson does not disclose an error correction code (ECC). However, Barth, Jr. discloses (see, for example, column 12, lines 10-34) a semiconductor memory device wherein fuses are programmed to perform an error correction. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to program the fuses of Macpherson and use them for error correction in order to remove the effects of bad bit lines in a memory device.

Response to Arguments

10. Applicant's arguments with respect to claims 2-12, 15-25, and 27 have been considered but are moot in view of the new ground(s) of rejection.

The whole semiconductor device may be construed as a "package." For example, a semiconductor device such as a PAL, FPGA or PLD which contain fuses may be called a package or any substrate (i.e. circuit board) it is put on may be called a package. See, for example, column 1, lines 46 until column 2, line 32 of Macpherson. Regarding the Crafts reference, see the abstract wherein Crafts states that a PROM device includes a fuse array formed on a substrate.

Regarding the Hamdy reference, the device is formed on a substrate (package) as shown in FIGURE 3. Also, FIGURE 5a clearly shows the anti-fuse 168h between the second end of anti-fuse 168d and output 178.

Regarding the Best reference, see, for example, column 2, lines 6-18.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee
October 29, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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